

**ELECTRONIC MEMORY CIRCUIT AND RELATED MANUFACTURING  
METHOD**

**Abstract of the Disclosure**

An electronic memory circuit comprises a matrix of EEPROM memory cells. Each memory cell includes a MOS floating gate transistor and a selection  
5 transistor. The matrix includes a plurality of rows and columns, with each row being provided with a word line and each column comprising a bit line organized in line groups so as to group the matrix cells in bytes, each  
10 of which has an associated control gate line. A pair of cells have a common source region, and each cell symmetrically provided with respect to this common source region has a common control gate region.